

CLAIMS

1. An input stage for an analog-digital converter, said stage comprising:

a buffer having an input terminal that receives an analog signal, and an output terminal;

a first switched capacitor circuit structure suitable for sampling the analog signal with a preset sampling period, the first switched capacitor circuit including first and second sampling switches coupled respectively with the output terminal and the input terminal of said buffer, said first and second sampling switches being controlled respectively by first and second signals to close respectively for a first interval of time and for a successive second interval of time of a first semi-sampling period of said sampling period; and

a second switched capacitor circuit structure connected to a reference voltage and to said buffer and suitable for generating said second signal with a voltage value greater in absolute value than the value of said analog signal for the duration of said second interval of time of the semi-sampling period.

2. The input stage according to claim 1, wherein said second switched capacitor circuit structure is connected to the input terminal of said buffer.

3. The input stage according to claim 1, wherein said second switched capacitor circuit structure is connected to the output terminal of said buffer.

4. The input stage according to claim 1 wherein the voltage value of said second signal is greater in absolute value than the voltage value of the analog signal by a quantity basically equal to the voltage value of said reference voltage.

5. The input stage according to claim 4 wherein said second switch is a transistor having a driving terminal and said second circuit structure comprises a capacitor, a third switch connected between a first terminal of said capacitor and said reference voltage, a fourth switch connected between the second terminal of said capacitor and ground, said third and fourth switches being controlled to close during a second semi-sampling period so as to load said capacitor at a voltage value basically equal to said reference voltage, a fifth switch connected to said input terminal of said buffer and to said first terminal of the capacitor and a sixth switch connected between said second terminal of the capacitor and the driving terminal of said transistor, said fifth and sixth switches being active during the second interval of time of the first semi-sampling period to obtain said second signal on said driving terminal of the transistor.

6. The input stage according to claim 4 wherein said second switch is a transistor having a driving terminal and said second circuit structure comprises a capacitor, a third switch connected between a first terminal of said capacitor and said reference voltage, a fourth switch connected between the second terminal of said capacitor and ground, said third and fourth switches being controlled to close during a second semi-sampling period so as to load said capacitor at a value of voltage substantially equal to said reference voltage, a fifth switch connected to said output terminal of said buffer and a said first terminal of the capacitor and a sixth switch connected between said second terminal of the capacitor and the driving terminal of said transistor, said fifth and sixth switches being active during the second interval of time of the first semi-sampling period to obtain said second signal on said driving terminal of the transistor.

7. A sample and hold stage for an analog-digital converter, the stage comprising:

a buffer having an input terminal that receives an analog signal, and an output terminal;

a first switched capacitor circuit structure suitable for sampling the analog signal during a sampling period, the first switched capacitor circuit including first and second sampling switches coupled respectively with the output terminal and the input terminal of the buffer; and

a second switched capacitor circuit structure connected to the buffer and including:

- a first capacitor having first and second electrodes;
- a first switch connected between the first electrode and a first reference voltage;

- a second switch connected between the second electrode and a second reference voltage;

- a third switch connected between the buffer and a first node between the first electrode and the first reference voltage; and

- a fourth switch connected between a control terminal of the second sampling switch and a second node between the second electrode and the second reference voltage.

8. The stage of claim 7 wherein the third switch is connected between the first node and the input terminal of the buffer.

9. The stage of claim 7 wherein the third switch is connected between the first node and the output terminal of the buffer.

10. The stage of claim 7 wherein the first sampling switch is controlled by a first signal that is active during a first interval of a first half of the sampling period, the third and fourth switches are controlled by a second signal that is active during a second interval of the first half of the sampling period, and the first and second switches are controlled by a third signal that is active during a second half of the sampling period.

11. The stage of claim 7 wherein the first switched capacitor circuit further includes:

a second capacitor having a first electrode, connected to the first and second sampling switches, and a second electrode;

a fifth switch connected between the second electrode of the second capacitor and an output of the stage;

a sixth switch connected between the first electrode of the second capacitor and a third reference voltage; and

a seventh switch connected between the second electrode of the second capacitor and a fourth reference voltage.

12. The stage of claim 11 wherein the first sampling switch is controlled by a first signal that is active during a first interval of a first half of the sampling period, the third and fourth switches are controlled by a second signal that is active during a second interval of the first half of the sampling period, and the first, second, fifth, and sixth switches are controlled by a third signal that is active during a second half of the sampling period.

13. The stage of claim 7 wherein the first switched capacitor circuit further includes a fifth switch connected between the first reference voltage and a third node between the fourth switch and the control terminal of the second sampling switch.

14. A method of driving a sampling stage of an analog-digital converter during a sampling period, the sampling stage including first and second sampling switches connected between an input terminal, which receives an analog input signal, and a first capacitor, the method comprising:

using a first signal to close the first sampling switch for a first interval of a first half of the sampling period;

generating a second signal with a voltage value greater in absolute value than the analog input signal

using the second signal to close the second sampling switch for a second interval of the first half of the sampling period.

15. The method of claim 14 wherein the generating step is performed by a switched capacitor circuit that includes a second capacitor, the generating step including applying a first reference voltage across the second capacitor and disconnecting the second capacitor from the input terminal and the second sampling switch during a second half of the sampling period, the second half occurring before the first half, and connecting the second capacitor between the input terminal and a control terminal of the second sampling switch during the first half such that the second signal is substantially equal in voltage to the analog input signal plus the first reference voltage.

16. The method of claim 15, further comprising connecting the first capacitor between a second voltage reference and an output of the sampling stage during the second half.